"RESPONSE UNDER 37 CFR 1.116-
EXPEDITED PROCEDURE EXAMINING
GROUP 2811"

0057-2362-2YY

#29/B
6-21-03
Paxton

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

SHIGENOBU MAEDA ET AL. : GROUP ART UNIT: 2811

SERIAL NO: 09/176,315 :

FILED: OCTOBER 22, 1998 : EXAMINER: CRANE, S.

FOR: METHOD OF DESIGNING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND RECORDING MEDIUM

AMENDMENT UNDER 37 C.F.R. §1.116

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

SIR:

Responsive to the Official Action mailed January 14, 2003, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend Claims 6, 9, 11, 12, 16, and 19 as shown in the attached marked-up copy to read as follows:

6. (Amended) A semiconductor device including an MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed